

| L Number | Hits | Search Text | DB | Time stamp |
|----------|-------|--|---|------------------|
| 1 | 16123 | tim\$4 near5 constraint | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:01 |
| 2 | 3046 | ((tim\$4 near5 constraint) and (clock near5 signal)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:01 |
| 3 | 61 | (((((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls.) and internal and external and test) and static) and relat\$6 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:01 |
| 4 | 39 | ((((((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls.) and internal and external and test) and static) and relat\$6) and multip\$6) and paramet\$5 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:01 |
| 5 | 367 | ((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:01 |
| 6 | 128 | ((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls.) and internal and external | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:01 |
| 7 | 86 | ((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls.) and internal and external and test | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:04 |
| 8 | 61 | ((((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls.) and internal and external and test) and static | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:01 |
| 9 | 46 | ((((((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls.) and internal and external and test) and static) and relat\$6) and multip\$6 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:01 |
| 10 | 59 | ((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls.) and internal and external and test and (eliminat\$4 or deletet\$4) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:05 |
| 11 | 43 | ((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls.) and internal and external and test and (eliminat\$4 or deletet\$4) and parameter | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:05 |
| 12 | 29 | ((tim\$4 near5 constraint) and (clock near5 signal)) and 716/\$.ccls.) and internal and external and test and (eliminat\$4 or deletet\$4) and parameter and boundar\$4 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2004/10/15 07:05 |

| | Document ID | Issue Date | Pages | Title | Current OR |
|----|-------------------------|------------|-------|--|------------|
| 1 | US 20040025129 A1 | 20040205 | 18 | System and methods for pre-artwork signal-timing verification of an integrated circuit design | 716/6 |
| 2 | US 20030233622 A1 | 20031218 | 84 | Method and apparatus for an asynchronous pulse logic circuit | 716/1 |
| 3 | US 20030208723 A1 | 20031106 | 68 | Automated processor generation system for designing a configurable processor and method for the same | 716/1 |
| 4 | US 20030009727 A1 | 20030109 | 90 | Circuit designing apparatus, circuit designing method and timing distribution apparatus | 716/1 |
| 5 | US 20020162086 A1 | 20021031 | 19 | RTL annotation tool for layout induced netlist changes | 716/18 |
| 6 | US 20020083398 A1 | 20020627 | 90 | Circuit designing apparatus, circuit designing method and timing distribution apparatus | 716/1 |
| 7 | US 6760888 B2 | 20040706 | 65 | Automated processor generation system for designing a configurable processor and method for the same | 716/1 |
| 8 | US 6732336 B2 | 20040504 | 81 | Method and apparatus for an asynchronous pulse logic circuit | 716/1 |
| 9 | US 6678871 B2 | 20040113 | 84 | Circuit designing apparatus, circuit designing method and timing distribution apparatus | 716/6 |
| 10 | US 6618834 B2 | 20030909 | 88 | Circuit designing apparatus, circuit designing method and timing distribution apparatus | 716/2 |
| 11 | US 6530073 B2 | 20030304 | 18 | RTL annotation tool for layout induced netlist changes | 716/18 |

| | Document ID | Issue Date | Pages | Title | Current OR |
|----|------------------|------------|-------|---|------------|
| 12 | US 6477683 B1 | 20021105 | 39 | Automated processor generation system for designing a configurable processor and method for the same | 716/1 |
| 13 | US 6421818 B1 | 20020716 | 80 | Efficient top-down characterization method | 716/18 |
| 14 | US 6378123 B1 | 20020423 | 81 | Method of handling macro components in circuit design synthesis | 716/18 |
| 15 | US 6295636 B1 | 20010925 | 82 | RTL analysis for improved logic synthesis | 716/18 |
| 16 | US 6292931 B1 | 20010918 | 81 | RTL analysis tool | 716/18 |
| 17 | US 6289498 B1 | 20010911 | 81 | VDHL/Verilog expertise and gate synthesis automation system | 716/18 |
| 18 | US 6289491 B1 | 20010911 | 80 | Netlist analysis tool by degree of conformity | 716/5 |
| 19 | US 6263483 B1 | 20010717 | 81 | Method of accessing the generic netlist created by synopsys design compiler | 716/18 |
| 20 | US 6205572 B1 | 20010320 | 79 | Buffering tree analysis in mapped design | 716/5 |
| 21 | US 6195593 B1 | 20010227 | 35 | Reusable modules for complex integrated circuit devices | 700/97 |
| 22 | US 6173435 B1 | 20010109 | 80 | Internal clock handling in synthesis script | 716/18 |
| 23 | US 5883814 A | 19990316 | 20 | System-on-chip layout compilation | 716/2 |
| 24 | US 5867399 A | 19990202 | 64 | System and method for creating and validating structural description of electronic system from higher-level and behavior-oriented description | 716/18 |

| | Document ID | Issue Date | Pages | Title | Current OR |
|----|-----------------|------------|-------|--|------------|
| 25 | US 5801958 A | 19980901 | 95 | Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information | 716/18 |
| 26 | US 5740347 A | 19980414 | 49 | Circuit analyzer of black, gray and transparent elements | 714/33 |
| 27 | US 5623418 A | 19970422 | 66 | System and method for creating and validating structural description of electronic system | 716/1 |
| 28 | US 5555201 A | 19960910 | 95 | Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information | 716/1 |
| 29 | US 5452239 A | 19950919 | 131 | Method of removing gated clocks from the clock nets of a netlist for timing sensitive implementation of the netlist in a hardware emulation system | 703/19 |

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore®
 RELEASE 1.8

 Welcome
 United States Patent and Trademark Office

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **3** of **1079782** documents.A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.**Refine This Search:**

You may refine your search by editing the current search expression or entering a new one in the text box.

☐ Check to search within this result set
Results Key:**JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard**1 Metastability behavior of CMOS ASIC flip-flops in theory and test***Horstmann, J.U.; Eichel, H.W.; Coates, R.L.;*

Solid-State Circuits, IEEE Journal of , Volume: 24 , Issue: 1 , Feb. 1989

Pages:146 - 157

[\[Abstract\]](#) [\[PDF Full-Text \(860 KB\)\]](#) **IEEE JNL**
2 Fuzzy time point compatibility reasoning for microprocessor system*Yuen, S.M.; Lam, K.P.;*

Computers and Digital Techniques, IEE Proceedings- , Volume: 146 , Issue: 1 , Jan. 1999

Pages:68 - 76

[\[Abstract\]](#) [\[PDF Full-Text \(828 KB\)\]](#) **IEE JNL**
3 Clock period optimization in a multiphase edge-clocked circuit constrained to a maximum number of phases*Fernandez, F.; Sanchez, A.;*

EUROMICRO 97. 'New Frontiers of Information Technology'. Short Contribution Proceedings of the 23rd Euromicro Conference , 1-4 Sept. 1997

Pages:184 - 189

[\[Abstract\]](#) [\[PDF Full-Text \(232 KB\)\]](#) **IEEE CNF**
[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved